A'cont

the pre-delay/post-delay/ comparison block 110 generates output signals Add_delay and Subtract_delay that are, in turn, fed back to the controllable delay chain block 100 so as to adjust the delay time.

Paragraph beginning at page 2, line 18:

A2

The pre-delay/post-delay comparison block 210 compares the delayed clock signal Delayed_clock with a reference clock signal Reference_clock so as to determine whether increasing or decreasing the delay time of the delayed clock signal Delayed_clock is necessary. As a result of the comparison process, the pre-delay/post-delay comparison block 210 produces output signals Add_delay_i and Sub_delay_i to a careful delay controller 220.

Paragraph beginning at page 3, line 12:

A3

As described above, the conventional delay locked loop of Fig. 2 is insensitive to noise at the state when the delayed locked loop normally operates and the locking is done. However, there is a disadvantage that it takes a very long time from an initial condition in which the locking is not caused to the locking: That is, since, in order to adjust the time delay, there must be at least two determination processes for the increase or decrease in the delay time generated by the pre-delay/post-delay comparison block 210, the time required for the locking may be much longer compared with that of using only one time of determination, as in the delay locked loop of Fig. 1.

Paragraph beginning at page 6, line 2:

A4

The delay locked loop comprises a controllable delay chain block 300 for adjusting a delay time of a clock in response to output signals Add_delay and Subtract_delay of an instant locking delay controller 320, a pre-delay/post-delay comparison block 310 for determining the need for increase or decrease of the delay time by comparing a delayed clock signal Delayed_clock output from the controllable delay chain block 300 with a reference clock signal Reference_clock, and the instant locking delay controller 320 for generating the output signals Add_delay and Subtract_delay by

A4 Amd'

using output signals Add_delay_i and Sub_delay_i of the pre-delay/post-delay comparison block 310, the delayed clock signal Delayed_clock and the reference clock signal Reference__clock, wherein the output signals Add_delay and Subtract_delay are used to control the increase and decrease of the delay time at the controllable delay chain block 300.

Paragraph beginning at page 6, line 18:

A5

Unlike the conventional delay locked loop described in Fig. 2, in the inventive delay locked loop shown in Fig. 3, the delayed clock signal Delayed_clock and the reference clock, signal Reference_clock are coupled to both the pre-delay/post-delay comparison block 310 and the instant locking delay controller 320 in parallel. Therefore, the instant locking delay controller 320 can check whether the locking is accomplished or not by comparing the delayed clock signal Delayed_clock and the reference clock signal Reference_clock.

Paragraph beginning at page 13, line 6:

A6

If the careful delay controller 410 is used as soon as the locking detector 430 determines that the locking is accomplished, the entire locking time may become longer. Therefore, information representing that the locking is achieved should be outputted after a given time. On the other hand, information representing that the locking is not accomplished should be outputted without any delay.

Paragraph beginning at page 13, line 13:

A7

In order to provide a signal representing an unlocked state without delay while providing a signal representing a locked state only after a given time, output block 800 may be used. Output block 800 receives the time delayed clock signal Delayed-clock and delays the output signal of the pre-delay/post-delay logic block 550 by one or more than one clock cycles. Further, if information showing that the locking is not accomplished at the pre-delay/post-delay logic block 550 is coupled thereto, the output